What is claimed is:

1. A method of testing a memory device by using a data processing unit having a memory device mounted thereon, said method comprising:

a step of supplying a memory device to be tested with a signal to be supplied said memory device; and

a step of checking relationship between output signals produced from said memory device and output signals produced from said memory device to be tested.

2. The method of testing a memory device according to claim 1, wherein:

a plurality of said memory devices to be tested are to be tested and said signals are supplied in parallel to said plurality of memory devices to be tested.

3. The method of testing a memory device according to claim 1, wherein:

said data processing unit has a control circuit connected to said memory device, said control circuit controlling an operation of said memory device.

4. The method of testing a memory device according to claim 1, wherein:

said checking step is adapted to check said output signals for agreement/disagreement.

5. The method of testing a memory device according to claim 1, wherein:

said signals to be supplied to said memory device include an address signal, a data signal, a clock signal and a control signal.

6. The method of testing a memory device according to

claim 1, wherein:

said signals supplied to said memory device to be tested is transferred by means of a pipeline system.

7. The method of testing a memory device according to claim 2, wherein:

said signals supplied in parallel to said plurality of memory devices to be tested are transferred by means of a pipeline system.

8. The method of testing a memory device according to claim 7, wherein:

said signals supplied by means of said pipeline system are distributed in a plurality of stages and supplied in parallel to said plurality of memory devices to be tested.

9. A method of manufacturing a memory device comprising:

a step of forming a semiconductor device having a memory; and

a step of supplying said memory of said semiconductor device with signals to be supplied to a first memory mounted on a data processing unit and checking relationship between signals output from said first memory and signals output from said memory of said semiconductor device.

10. The method of manufacturing a memory device according to claim 9, wherein:

a plurality of said memories used in said step of forming said semiconductor device are to be formed and said signals to be supplied to said first memory are supplied in parallel to said plurality of memories used in said step of forming said semiconductor device.

11. The method of manufacturing a memory device

according to claim 9, wherein:

said data processing unit is coupled to said first memory and has a control circuit for controlling an operation of said first memory.

12. The method of manufacturing a memory device according to claim 9, wherein:

said checking step is adapted to check said output signals for agreement/disagreement.

13. The method of manufacturing a memory device according to claim 9, wherein:

said signals to be supplied to said first memory include an address signal, a data signal, a clock signal and a control signal.

14. An apparatus for testing a memory device, said apparatus comprising:

a socket to be mounted with a memory device to be tested;

a terminal supplied from a data processing unit mounted with a memory with signals to be supplied to the memory and output signals of said memory; and

a control section for determining relationship between the output signals of from said socket and the output signals from said memory.

15. The apparatus for testing a memory device according to claim 14, further comprising:

a first board for carrying said socket to be mounted with said memory device to be tested; and

a second board adapted to carrying a plurality of said first boards, distribute the signals to be supplied to said memory and supply the signals to said memory device to be

tested.

16. The apparatus for testing a memory device according to claim 15, wherein:

the apparatus comprises a plurality of types of said first boards to accommodate said memory device to be tested.

17. The apparatus for testing a memory device according to claim 16, wherein:

said memory device to be tested is a TSOP or a TCP.

18. The apparatus for testing a memory device according to claim 14, wherein:

a plurality of said memory devices to be tested are to be tested and said signals to be supplied to said memory are supplied in parallel to said plurality of memory devices to be tested.

19. The apparatus for testing a memory device according to claim 14, wherein:

said data processing unit is coupled to said memory and comprise a control connector for controlling an operation of said memory.

20. The apparatus for testing a memory device according to claim 14, wherein:

said control circuit is adapted to check said signals for agreement/disagreement.

21. The apparatus for testing a memory device according to claim 14, wherein:

said signals to be supplied to said memory include an address signal, a data signal, a clock signal and a control signal.

22. The apparatus for testing a memory device according

to claim 14, further comprising:

a substrate for taking out signals from the memory mounted on said data processing unit and supplying them to said terminal.

23. A method of testing a memory module by using a data processing unit mounted with a memory module having a plurality of memory devices, said method comprising:

a step of supplying a memory device to be tested with signals to be supplied to said memory module; and

a step of checking the relationship between output signals from said memory module and output signals from said memory device to be tested.

24. The method of testing a memory module according to claim 23, wherein:

said signals to be supplied to said memory module are signals to be supplied to a first memory device of said plurality of memory devices and said output signals from said memory module are the output signals from a second memory device of said plurality of memory devices.

25. The method of testing a memory module according to claim 24, wherein:

said first memory device and said second memory device may be a same memory device.

26. The method of testing a memory module according to claim 23, wherein:

a plurality of said memory devices to be tested are to be tested and said signals to be supplied to said memory module are supplied in parallel to said plurality of memory devices to be tested.

27. The method of testing a memory module according to claim 23, wherein:

said data processing unit is coupled to said memory module and has a control circuit for controlling an operation of said memory module.

28. The method of testing a memory module according to claim 23, wherein:

said checking step is adapted to check said output signals for agreement/disagreement.

29. The method of testing a memory module according to claim 23, wherein:

said signals to be supplied to said memory module include an address signal, a data signal, a clock signal and a control signal.

30. The method of testing a memory module according to claim 23, wherein:

said memory device to be tested is one of a plurality of memory devices mounted on memory module.

31. A method of manufacturing a memory module comprising:

a step of preparing a memory device;

a step of supplying said memory device, from a data processing unit mounted with a first memory, with signals to be supplied to the first memory and checking relationship between output signals from said first memory and output signals from said memory device; and

a step of forming the memory module by mounting on a substrate said memory device checked for the relationship in the preceding step.

32. The method of manufacturing a memory module according to claim 31, wherein:

a plurality of said memory devices are prepared and said signals to be supplied to said first memory are supplied in parallel to said plurality of memory devices.

33. The method of manufacturing a memory module according to claim 31, wherein:

said data processing unit is coupled to said first memory and has a control circuit for controlling an operation of said memory module.

34. The method of manufacturing a memory module according to claim 31, wherein:

said checking step is adapted to check said output signals for agreement/disagreement.

35. The method of manufacturing a memory module according to claim 31, wherein:

said signals to be supplied to said first memory include an address signal, a data signal, a clock signal and a control signal.

36. An apparatus for testing a memory module, said apparatus comprising:

a board to be provided with a memory module having a plurality of memory devices;

a terminal supplied from a data processing unit mounted with said memory module with signals to be supplied to the memory module and with output signals of said memory; and

a control section for supplying said board with signals to be supplied to said memory module, and for determining relationship between output signals from said board and output

signals from said memory module.

37. The apparatus for testing a memory module according to claim 36, wherein:

said signals to be supplied to said memory module are signals to be supplied to a first memory device of said plurality of memory devices and said output signals from said memory module are output signals from a second memory device of said plurality of memory devices.

38. The apparatus for testing a memory module according to claim 37, wherein:

said first memory device and said second memory device may be a same memory device.

39. The apparatus for testing a memory module according to claim 36, wherein:

said signals to be supplied to said memory module are supplied in parallel to said plurality of memory devices.

40. The apparatus for testing a memory module according to claim 36, wherein:

said data processing unit is coupled to said memory module and has a control circuit for controlling the operation of said memory module.

41. The apparatus for testing a memory module according to claim 36, wherein:

said control section is adapted to check said output signals for agreement/disagreement.

42. The apparatus for testing a memory module according to claim 36, wherein:

said signal to be supplied to said first memory include an address signal, a data signal, a clock signal and a control

signal.

43. The apparatus for testing a memory module according to claim 36, wherein:

said apparatus for testing a memory module is adapted to define a test unit on said board.

44. The apparatus for testing a memory module according to claim 43, wherein:

one of said plurality of memory devices mounted on said memory module to be provided on said board is tested.

45. A method of manufacturing a computer comprising:

a step of preparing a mother board carrying a CPU, a socket to be mounted with a memory device to be tested and a control circuit connected to said CPU and said socket;

a step of preparing a memory module having a plurality of memory devices; and

a step of arranging said memory module on said socket;

said memory devices of said memory module satisfying a predetermined relationship in a test step;

said test step being adapted to supply said memory devices, from a data processing unit mounted with a first memory, with signals to be supplied to said first memory, and adapted to check relationship between output signals from said first memory and output signals from said memory devices.

46. The method of manufacturing a computer according to claim 45, wherein:

said signals to be supplied to said first memory are supplied in parallel to said plurality of memory devices.

47. The method of manufacturing a computer according to claim 45, wherein:

said data processing unit is coupled to said first memory and has a control circuit for controlling an operation of said first memory.

48. The method of manufacturing a computer according to claim 45, wherein:

said checking step is adapted to check said output signals for agreement/disagreement.

49. The method of manufacturing a computer according to claim 45, wherein:

said signals to be supplied to said first memory include an address signal, a data signal, a clock signal and a control signal.

50. A method of testing a memory module having a data processing unit provided with a DIMM carrying a plurality of memory devices, said method comprising;

a step of supplying said memory devices to be tested with signals to be supplied said DIMM: and

a step of checking relationship between output signals produced from said DIMM and output signals produced from said memory devices to be tested.

51. A method of manufacturing a memory device comprising:

a step of preparing a memory device;

a step of supplying said memory device from a data processing unit carrying a first memory with signals to be supplied to said first memory and checking relationship between signals output from said first memory and the signal output from said memory device; and

a step of forming a DIMM by mounting on a substrate the

memory device checked in the above step for a predetermined relationship.

52. An apparatus for testing a memory module, said apparatus comprising:

a board to be provided with a DIMM carrying a plurality of memory devices;

a terminal supplied from a data processing unit mounted with a DIMM with signals to be supplied to the DIMM and with output signals from said DIMM; and

a control section adapted to supply said board with said signals to be supplied to said DIMM for determining relationship between output signals from said board and output signals from said DIMM.

53. A method of manufacturing a computer comprising:

a step of preparing a mother board carrying a CPU, a socket to be mounted with a DIMM, and a control circuit connected to said CPU and said socket;

a step of preparing a DIMM carrying a plurality of memory devices; and

a step of arranging said DIMM on said socket;

said memory devices of said DIMM satisfying a predetermined relationship in a test step; and said test step being adapted to supply said memory devices with signals from a data processing unit mounted with a first memory, said signals being to be supplied to said first memory, and adapted to check relationship between output signals from said first memory and output signals from said memory devices.